REMARKS

Claims 18-29 are in pending in the application and stand rejected. Claims 18 and 23 have been amended. New claims 30-34 have been added. No new matter has been introduced by virtue of the claim amendments and additions. The Examiner's reconsideration of the claim rejections is respectfully requested.

Claim Rejections -35 USC § 103

Claims 18-29 stand rejected under 35 USC § 103 as being unpatentable over Kasai et al., EP 684,637A3 (Kasai) in view of Ho et al., US 5,643,823 (Ho).

To establish a prima facie case of obviousness based on the combination of Kasai and Ho, various criteria must be met. For instance, the combination of Kasai and Ho *must* teach or suggest all the claim limitations. Further, there must be some suggestion or motivation in the references or in the knowledge generally available to one skilled in the art to combine their teachings. The teaching or suggestion to make the claimed combination must both be found in the prior art and not based on *hindsight* in view of applicant's disclosure (see, e.g., MPEP 2141, 2143, 2143.03).

It is respectfully submitted that at the very minimum, the combination of Kasai and Ho is legally deficient to establish a prima face case of obviousness against claims 18, 23 and 30. For instance, with respect to claim 18, 23 and 30, neither Kasai nor Ho, singularly or in combination, discloses or suggests *a trench capacitor comprising a dielectric stack having a* ***continuous monocrystalline silicon nitride layer***, as essentially claimed in claims 18, 23 and 30. Furthermore, with respect to claims 18 and 23 neither Kasai nor Ho, singularly or in combination, discloses or suggests *a trench capacitor comprising a dielectric stack having a*

continuous monocrystalline silicon nitride layer *that is formed* ***on hydrogen baked surfaces*** *of trenches in a silicon substrate*, as essentially claimed in claims 18 and 23.

In the Final Office Action of November 6, 2001, Examiner acknowledges that Kasai does not disclose a crystalline silicon nitride layer (much less a *continuous monocrystalline silicon nitride layer* as claimed). Indeed, Kasai discloses a method for simultaneously removing natural oxide from surfaces of a trench while forming a thermal nitride film. Although Kasai discloses removing the natural oxide from the trench surfaces, *the resulting silicon nitride film contains oxygen impurities* (see, e.g., Col. 16, lines 14-45 (claims 1, 6 and 7)).

It is respectfully submitted that Ho does not cure the deficiencies of Kasai in that Ho does not disclose or suggest *a continuous monocrystalline silicon nitride layer formed on trenches surfaces of a silicon substrate, wherein the surfaces are substantially free of oxide.* Indeed, in stark contrast, Ho discloses a process of (i) forming a STI trench, (ii) forming an ***oxide*** *layer on the trench surfaces* (see, e.g., Fig. 1A), (iii) LPCVD depositing an amorphous silicon nitride layer (Fig. 1B, col. 2, lines 59-60), and then performing rapid thermal annealing of the amorphous silicon nitride film to form a "crystallized" silicon nitride film that is largely crystalline (Fig. 1C, col. 3, lines 9-10).

Thus, Ho does not disclose a process that forms a continuous monocrystalline silicon nitride film, much less a continuous monocrystalline silicon nitride film that acts a dielectric for a trench capacitor, as essentially claimed in claims 18, 23 and 30. Indeed, Ho does not disclose or suggest that further annealing or higher temperatures would ultimately result in a continuous monocrystalline silicon nitride film. Furthermore, to the extent that Ho specifically discloses forming the silicon nitride layer *on an oxide film*, this teaches away from the claim invention

wherein a continuous monocrystalline silicon nitride layer is formed on an oxide-free silicon surface of the trench.

Furthermore, with respect to claims 18 and 23, the combination of Kasai and Ho does not disclose or suggest *a trench capacitor comprising a dielectric stack having a continuous monocrystalline silicon nitride layer that is formed on* ***hydrogen baked surfaces of trenches*** *in a silicon substrate*, as essentially claimed in claims 18 and 23. Indeed, although Kasai discloses a process of removing native oxide from the surfaces, Kasai does not disclose or suggest hydrogen baking the silicon surfaces of the trench. Furthermore, Ho expressly discloses forming an *oxide layer on the trench surface prior to forming silicon nitride.* Thus, the combination does not disclose or suggest hydrogen baked trench surfaces.

Thus, for at least the reasons given above, the combination of Kasai and Ho fails to teach or suggest elements of claims 18, 23 and 30.

Furthermore, it is respectfully submitted that there is no objective motivation or suggestion to combine the teachings of Kasai and Ho. In the Final Office Action, Examiner states (page 4) that "one of ordinary skill in the art, at the time of the invention, would have found it obvious to arrive at the presently claimed limitations as it would have been obvious to one of ordinary skill in the art that the thermal nitride of Kasai would be in crystalline form, as the Ho reference discloses that a silicon nitride film produced by high temperature exposure to ammonia is in crystalline form." Examiner further states (page 5) that Ho "is simply relied on to show that a nitride layer made by the process of Kasai would result in a crystalline nitride layer."

It is respectfully submitted that Examiner's conclusions of obviousness are legally flawed for several reasons. To begin, Examiner has failed to explain how the process of Ho could be

applied in the Kasai process to form a continuous monocrystalline crystalline silicon nitride layer from an amorphous silicon nitride layer containing oxygen impurities. Indeed, as noted above, Kasai discloses a process of forming an amorphous thermal nitride film under conditions in which *oxygen impurities* are included in the film as a result of simultaneously removing the native oxide. In contrast, Ho discloses a method of forming an amorphous CVD silicon nitride film, and then rapid thermal annealing the amorphous film to crystallize the film. Ho does not teach reaction conditions that would contaminate the initial amorphous CVD nitride layer with impurities such as oxygen. In any event, there is nothing in Ho to suggest that the rapid thermal annealing of an amorphous silicon nitride layer contaminated with impurities would result in a crystalline silicon nitride layer.

Furthermore, notwithstanding that Ho discloses a method for crystallizing an amorphous silicon nitride layer, Ho is directed to a method for forming silicon nitride liners for STI structures, wherein the silicon nitride liner acts as an O_2 barrier (see, e.g., Abstract). Ho is not specifically related to methods for forming trench capacitors, much less a node dielectric layer that comprises a continuous monocrystalline silicon nitride film. Although Kasai is related to trench capacitors, Kasai discloses forming an amorphous silicon nitride layer as a node dielectric. Thus, one of ordinary skill in the art would not be motivated to combine the teachings of Kasai and Ho to derive the inventions of claim 18, 23 and 30.

For at least all the above reasons, claims 18, 23 and 30 are believed to be patentable and non-obvious over the combination of Kasai and Ho. In addition, all claims that depend from claims 18, 23 and 30 are believed to be patentable and non-obvious over the combination of Kasai and Ho at least by virtue of their dependence from respective base claims 18, 23 and 30.

For all of the foregoing reasons, Applicant believes the claims are in condition for

allowance. f the Examiner is relying on any personal knowledge in rejecting any claims, Applicants respectfully request that any such knowledge be made known to Applicants in an affidavit in accordance with 37 C.F.R §1.107.

Respectfully submitted,

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